

plurality of main word lines being allotted to one of said plurality of sets of sub-word lines;

a plurality of second regions, each of which is arranged alternately with each of said first regions arranged along said first direction and each of which includes sub-word line drivers connected to said sub-word lines;

01 a plurality of third regions, each of which is arranged alternately with each of said first regions arranged along said second direction and each of which includes sense amplifiers connected to said data lines; and

a plurality of fourth regions, each of which is arranged alternately with each of said third regions arranged along said first direction,

wherein each of said plurality of main word lines extends through one or more of said first regions arranged along said first direction;

wherein said semiconductor memory further includes:

a plurality of pairs of sub-common data lines, each of which extends in said first direction through said third regions arranged along said first direction;

first switching circuits formed in said third regions and connected interposingly between said plurality of pairs of data lines and a corresponding one of said pairs of sub-common data lines;

a plurality of pairs of main-common data lines, each of which extends in said second direction through one or more of second regions arranged along said second direction; and

second switching circuits formed in said fourth regions and connected interposingly between a corresponding one of said pairs of main-common data lines and a corresponding one of said pairs of sub-common data lines.

2. [A] The semiconductor memory according to claim 1,

wherein a number of memory arrays allotted to one of said main word-lines is greater than a number of memory arrays allotted to a corresponding one of said pairs of sub-common data lines.